RESEARCH ARTICLE OPEN ACCESS

Design the High Speed Kogge-Stone Adder by Using

MUX

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Abstract
In this Technical era the high speed and low area of VLSI chip are very- very essential factors. Day by day number of transistors and other active and passive elements are growing on VLSI chip. In Integral part of the processor adders play an important role. In this paper we are using proposed kogge-stone adders for binary addition to reduce the size and increase the efficiency or processors speed. Proposing kogge stone adder provides less components, less path delay and better speed compare to other existing kogge stone adder and other adders. Here we are comparing the kogge stone adders of different-different word size from other adders. The design and experiment can be done by the aid of Xilinx 14.1i Spartan 3 device family.

Keywords: Kogge Stone Adder, Ripple Carry Adder, Proposed Kogge Stone Adder, 14.1i Spartan 3 Device Family.

I. INTRODUCTION

The stage of multiplication in any crucial appli-cation considered greatly influence the processor speed. The processors speed mostly depends on adder design techniques. Adder is the device by which two or more than two bit information can be added. These devices are need of hour for dig-ital signal processing and image signal processing. Vedic mathematics is the best option to calculate the fast asthmatics and logical operation in fast way. There are 16 sutras in vedic mathematics like urd-hawa triyakbhayam, Nikhilam etc. So we are kept in mind that reduce the area and logical path delay as possible as. The propagation delay is played a very important role for digital signal processing, image processing and other various suitable appli-cation..The shorter the propagation delay, the higher the speed of the circuit and vice-versa. Propagation delay should be minimizing as possible as, for high efficient addition. For better explanation we can take instance for N bit addition in which generally propagation delay is occurred highly. When we add one high bit information(A0; A1; A2; A3) to another high bit information(B0; B1; B2; B3), carry bit(C0; C1; C2; C3) is occurred due to normally binary addition operation. This carry propagates to next bit and now bit addition is performed by 3 bit adder. So carry will propagate to the next bit over and over, this cause propagation delay will be occurred. We have principal component for 2 and 3 bit addition such as half and full adder. There another serial and parallel adder to design fast processing adder like compressor, Ripple carry adder, look a head adder etc.

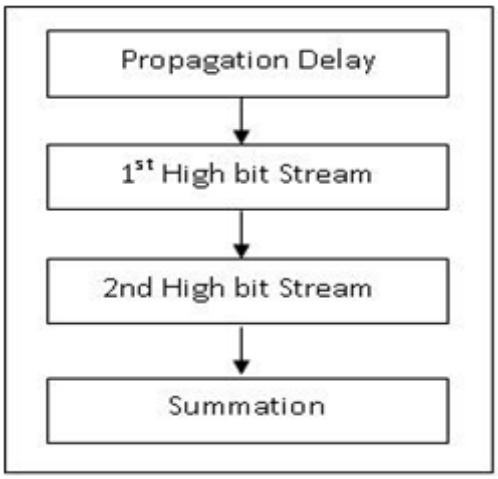

Fig. 1. A Propagation delay for bit binary addition

II. OBJECTIVE

The bottleneck motive the work is to design and implement a high speed adder. Which can be used in any processor based application. Here we are proposing a Kogge stone adder (KSA) by using MUX to reduce the propagation delay.

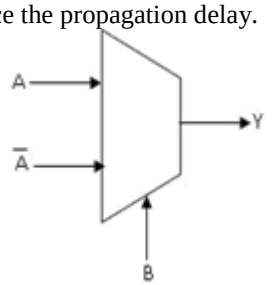

Fig. 2. A MUX blockdiagram for working as a XOR gate

III. MUX AS A XOR GATE

XOR gate is the special type of gate which is represented by plus sign with encirclement. The

matter of complexity can be reduced by the aid of designing of the gates. Less number of gates provides the less area for attractive designing in digital processing. Xor gate is comprised with five gates (Two AND, two NOT and one OR gate). XOR gate can also be replaced by Multiplexer (MUX). In digital electronics we are having two types of universal gates like NAND and NOR gate. By using any universal gate we can design any type of gate. Likewise MUX behaves like as universal gate that means by using mux any type of gate can be designed. To design the 2 inputs XOR gate one input of MUX must be invert to the other and both input would be connected together. Another input of XOR gate would be applied to the select line of the MUX.

So, the output of the MUX would be as same as the output of XOR Gate. The advantage of this type of designing that is Differential Cascode Voltage Switch Logic (DCVSL) as a MUX is that it produces both true and complementary outputs when provided with true and complementary inputs.

IV. DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC (RCA)

A ripple carry adder is a parallel digital adder circuit that produces the arithmetic sum of two binary numbers. It can be comprised with full adders connected in cascaded, with the carry output from each full adder connected to the carry input of the next full adder in the chain. This kind of adder is typically known as Ripple Carry Adder because carry ripples to next full adder. The layout of Ripple Carry Adder is simple, which allows fast design

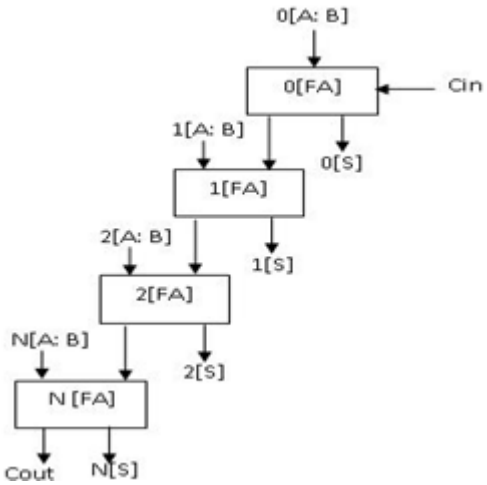

Fig. 3. A Functional Diagram of Ripple Carry Adder

time. The Ripple Carry Adder is slowest among all the adders because every full adder must wait till the previous full adder generates the carry bit for its input.

$$S_0 = A_0B_0C_{in} \quad (1)$$

$$C_0 = (A_0B_0) + (B_0C_{in}) + (C_{in}A_0) \quad (2)$$

$$S_1 = A_1B_1C_0 \quad (3)$$

$$C_1 = (A_1B_1) + (B_1C_0) + (C_0A_1) \quad (4)$$

$$S_2 = A_2B_2C_1 \quad (5)$$

$$C_2 = (A_2B_2) + (B_2C_1) + (C_1A_2) \quad (6)$$

$$S_n = A_nB_nC_{n\ 1} \quad (7)$$

$$C_n = (A_n B_n) + (B_n C_{n\ 1}) + (C_{n\ 1}A_n) \quad (8)$$

The ripple carry adder has the smallest are when compare to other adder. it is limited to application where the area and propagation delay must be minimized. As we can see in diagram of ripple carry adder which has much more number of gates. Ripple carry adder does not provide efficient area and speed because of its complexity.

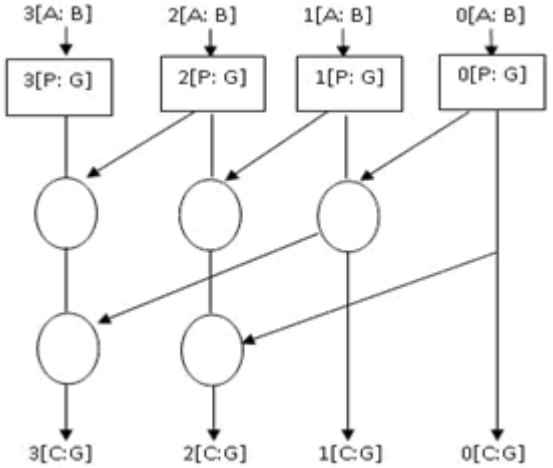

Fig. 4. A Basic Building Block of KSA

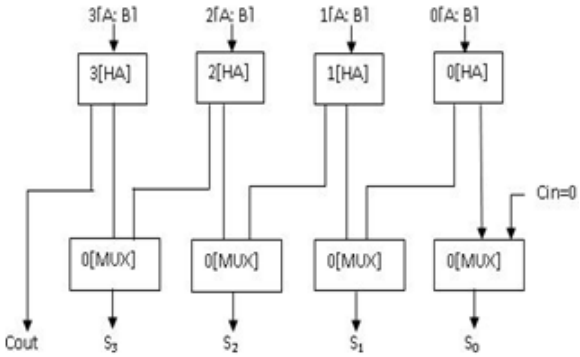

Fig. 5. Proposed KSA by using MUX

V. KOGGE-STONE ADDER

The Kogge-Stone adder concept was developed by Peter M. Kogge and Harold S. Stone, which they published in 1973 in a seminal paper titled. KS adder is the special and fast adder. Kogge stone adder is comprised with three units such as pre processing, carry generator and post processing unit.

$$P = A_iB_i \quad (9)$$

$$G = A_iB_i \quad (10)$$

$$C_i = G_i \quad (11)$$

$$S_i = P_iC_{i\ 1} \quad (12)$$

In kogge stone adder XOR can be replaced by MUX which provide different structure and gives the true and complement value at a time.

TABLE I
COMPRESION OF DIFFERENT TYPES OF ADDER WITH KSA BY MUX

Bit size	Adder	Area	Delay in ns
8 bit	Regular(RCA)	144	11.92
SQRT	BEC	132	13.69
CSLA	Modified (CBL)	111	11.15
	KSA by MUX	83	5.776
16 bit	Regular (RCA)	348	16.15
SQRT	BEC	291	18.77
CSLA	Modified (CBL)	276	15.48
	KSA by MUX	166	12.85
32 bit	Regular (RCA)	698	28.97
SQRT	BEC	762	34.44
CSLA	Modified (CBL)	552	26.23
	KSA by MUX	332	24.56
64 bit	Regular (RCA)	1592	52.82
SQRT	BEC	1498	64.61
CSLA	Modified (CBL)	1104	47.74
	KSA by MUX	664	45.25

VI. CONCLUSION AND FUTURE WORK

Eventually a novel high speed adder can be implemented by different structure of kogge stone adder. Simulation result is implementing on Xilinx 14.2i Spartan 3E advanced VHDL software tool. This experiment gives better result than other adder apart from that it gives less area and low propagation delay. In future this adder can be helped to design a high speed multiplier which is essential for digital processor. Apart from that these fast adder and multiplier can be used for convolution and de-convolution.

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